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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,754	08/13/2001	Ralph C. Taylor	00100010064	8666

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,754	TAYLOR ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed May 07, 2004, with respect to the rejections of claims 1-19 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Niu et al. (U.S. Patent No. 6,268,874).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 7-15, and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Niu et al. (U.S. Patent No. 6,268,874).

Referring to claims 1 and 13, Niu et al. teach a method for processing graphics, wherein as shown in Fig. 3, graphics data are transmitted on a bus 212 to the graphics engine 204. Graphics data are preferably pixel or primitive information retrieved from the frame buffer 202. Graphics data are processed in accordance with instructions received from the processor 208 (communication between a host processor with a graphics processor). Niu et al. also teach the pixel information contain primitive information and state information. State information denote the type of processing that is to be done on the primitive (a least one set of state data is used to process graphics

primitives) (col. 3, lines 49-67, and col. 4, lines 1-22). Niu et al. further teach shadow stages 412 comprise registers 410 for holding state data 480 (buffer for receiving and storing state data) (col. 5, lines 32-33). The depth of the shadow stages 412 for each processing element 464 in a processing stage changes incrementally. For the first processing element 464 in a processing stage, the depth is assigned to be one. Then, the depth for the next processing element 464 is incremented by one, and so on. This pattern increases with the number of processing elements 464, so that if there are N processing elements 464, there must be N+1 shadow stages 412 and corresponding valid bits 414 for the processing elements 464 (total length of N sets of state data does not exceed a length of the buffer) (Fig. 4, and col. 6, lines 41-62). With reference to Fig. 5, Niu et al. teach if the register write is for the setup unit 400, the controller 420 determines whether there is space available in the shadow stages 412 to receive the new state information 480 (step 514). If there is not, the controller 420 waits until a slot opens, and the pipeline 100 stalls (step 530) (col. 7, lines 7-12), thus prohibiting an additional set of state data from being stored in the buffer when N equals to a maximum number of allowed states.

In regard to claims 2 and 14, Niu et al. teach for the second processing element 464, a shadow stage 412 must be added in order to be able to store the state data 480 for the first primitive data 484 group while it is being processed by the first processing element 464, and the state data 480 for the second primitive group as it is transmitted down the state data stream 480 (col. 6, lines 50-56). Therefore, in this case, the maximum number of allowed states is two.

Referring to claims 3 and 15, as shown in Fig. 7, Niu et al. teach pon receiving a new state, the state controller 420 determines whether the one shadow stage 412

(associated with the Chubbie) processing element 464 is available. If it is not, the pipeline 100 stalls until all of the primitives have been processed corresponding to the states represented by the dirty bits 415 and the one shadow stage 412. Once the shadow stage 412 is available, the new state is loaded and the pipeline 100 begins transmitting new primitive information again (permitting additional set of state data to be stored in the buffer when (determining) M sets of state data are no longer being used to process the graphics primitives) (col. 7, lines 64-67, and col. 8, lines 1-5) (in this example, the examiner assumes M = N = 1).

In regard to claim 4, as cited above, Niu et al. shadow stages 412 (a constant buffer) comprise registers 410 for holding state data 480 (constant state data).

Referring to claims 5 and 16, as cited above, Niu et al. teach a method for storing state data in a buffer, wherein the total length of N sets of state data does not exceed a length of the buffer. Niu et al. further teach determining whether a length of an additional set of state data would exceed available space in the buffer by checking available space in the shadow stage 412 as shown in Fig. 5 and as cited above. As shown in Fig. 8, Niu et al. further teach if the dirty bit 415 is marked, which indicates that the state for the next primitive is different then the state for the current primitive, the primitive controller 424 blocks incoming pixels from being transmitted into the processing element 464. After receiving an EOP_E token, which means that the current operating primitive has been flushed out of the processing element, the controller 424 then moves to the Idle state 800 and waits for the first shadow register to be validated (thus, waiting until M sets of state data no longer used to process graphics primitives). When the shadow register is validated, the primitive controller 424 shifts into the

processing state 804, and the new state is loaded into the working registers and the next primitive is processed. By waiting for the previous primitive to be flushed before loading the new state, the controller ensures that the primitives are only processed in accordance with their correct state (col. 8, lines 41-55). Since the size of the buffer (shadow stage 412) can be limited as in the example shown on column 7, lines 60-67 and column 8, lines 1-5, new state data can overwrite the previous state data in the buffer.

In regard to claims 7, 8, 18 and 19, as cited above, Niu et al. teach the number of sets of state data can be two. As also cited above, Niu et al. teach waiting until all sets of state data to finish processing graphics primitives before loading new state.

In regard to claim 9, Niu et al. teach if the dirty bit 415 (a flush command) is marked, which indicates that the state for the next primitive is different then the state for the current primitive, the primitive controller 424 blocks incoming pixels from being transmitted into the processing element 464 (Fig. 8, and col. 8, lines 41-45).

Referring to claim 10, as cited above, Niu et al. the buffer is a constant buffer.

In regard to claims 11 and 12, as cited above, Niu et al. teach graphics data are processed in accordance with instructions received from the processor 208 (a host). Thus, graphics data and instructions are stored in the host processor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Niu et al. (U.S. Patent No. 6,268,874) in view of admitted prior art.

Referring to claim 6 and 17, as applied to claim 5 and 16 above, Niu et al. teach a buffer for storing state data, and thus, Niu et al. teach all the limitations of claims 6 and 17, except that the buffer is a ring buffer. However, as admitted to prior art, ring buffer are well known in the art (page 9 of the application).

Therefore, it would have been obvious to one skilled in the art to implement the buffer as taught by Niu et al. as a ring buffer so that input data can be wrapped to the beginning of the buffer when its end is reached, thus saving time and increase the speed.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

07/13/2004

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600